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Number of Pages (including this page)

Date: May 3, 2004  
To: Annette M. Thompson - 2825  
Location: United States Patent and Trademark Office  
Fax No.: (703) 872-9306  
From: Michael P. Noonan - 42,038  
Subject: 10/025,289- Andrew K. Martin et al.

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## MESSAGE:

Enclosed herewith, please find a FORMAL AMENDMENT for filing in the below-identified application. If Applicant has overlooked any fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit 503079, Freescale Semiconductor, Inc.

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EXAMINER: Annette M. Thompson  
GROUP ART UNIT: 2825  
SERIAL NO.: 10/025,289  
FILED: DECEMBER 19, 2001  
INVENTOR: ANDREW K. MARTIN ET AL.

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UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S) Andrew K. Martin et al. GROUP ART UNIT: 2825  
APPLN. NO.: 10/025,289 EXAMINER: Annette M. Thompson  
FILED: December 19, 2001  
TITLE: DESIGN VERIFICATION SYSTEM FOR AVOIDING FALSE  
FAILURES AND METHOD THEREFOR

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RESPONSE TO FINAL REJECTION

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Responsive to the Office Action dated March 3, 2004, and Examiner's comments with  
regard thereto, please enter the following amendments in the above-entitled application, without  
prejudice or disclaimer.